Dynamic range of Zyla and Neo sCMOS cameras

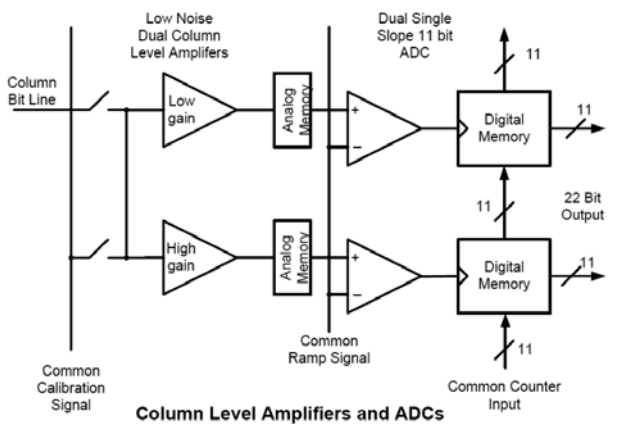## Unique dual amplifier dynamic range sCMOS sensor

Figure 1 - Schematic layout of sCMOS columns level amplifiers and analogue to digital converters (ADCs)

The Dual Amplifier architecture of sCMOS sensor in Neo and Zyla uniquely circumvents the need to choose between low noise or high well capacity, in that signal can be sampled simultaneously by both high gain and low gain amplifiers respectively. As such, the lowest noise of the sensor can be harnessed alongside the maximum well depth, affording the widest possible dynamic range.

Traditionally, scientific sensors including CCD, EMCCD, ICCD and CMOS, demand that users must select 'upfront' between high or low amplifier gain (i.e. sensitivity) settings, depending on whether they want to optimise for low noise or maximum well depth. Since the true dynamic range of a sensor is determined by the ratio of well depth divided by the noise floor detection limit, then choosing either high or low gain settings will restrict dynamic range by limiting the effective well depth or noise floor, respectively.

For example, consider a large pixel CCD, with 16-bit Analogue to Digital Converter (ADC), offering a full well depth of 150,000 e⁻ and lowest read noise floor of 3 e⁻. The gain sensitivity required to give lowest noise is 1 e⁻/ADU (or 'count') and the gain sensitivity required to harness the full well depth is 2.3 e⁻/ADU, but with a higher read noise of 5 e⁻. Therefore, it does not automatically follow that the available dynamic range of this sensor is given by 150,000/3 = 50,000:1. This is because the high sensitivity gain of 1e⁻/ADU that is used to reach 3 e⁻ noise means that the 16-bit ADC will top out at 65,536 e⁻, well short of the 150,000 e⁻ available from the pixel. Therefore, the actual dynamic range available in 'low noise mode' is 65,536/3 = 21,845:1. Conversely, the lower sensitivity gain setting means that the ADC will top out at ~ 150,000 e⁻, but the higher read noise of 5 e⁻ will still limit the dynamic range to 150,000/5 = 30,000:1 in this 'high well depth mode'.
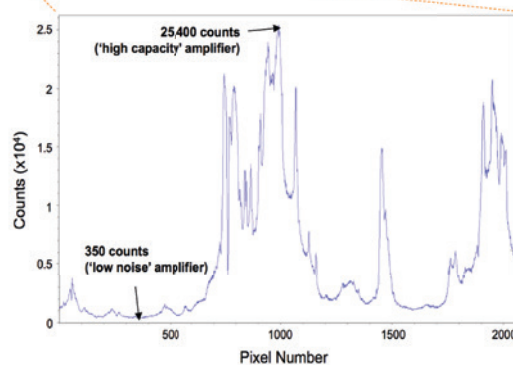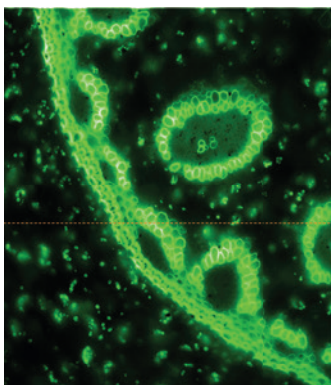

Figure 2 - High contrast image, of labeled fixed cell, due to the dual amplifier architecture of sCMOS providing a 16-bit data range. Intensity line profile shows signal at high counts, being sampled by the high capacity (low gain) amplifier, and signal at low counts, being sampled by the low noise (high gain) amplifier.

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sCMOS sensor offers a unique dual amplifier architecture, meaning that signal from each pixel can be sampled simultaneously by both high and low gain amplifiers. The sensor also features a split readout scheme in which the top and bottom halves of the sensor are read out independently. Each column within each half of the sensor is equipped with dual column level amplifiers and dual analog-to-digital converters, represented as a block diagram in Figure 1. The dual column level amplifier/ADC pairs have independent gain settings, and the final image is reconstructed by combining pixel readings from both the high gain and low gain readout channels to achieve a wide intra-scene dynamic range, uniquely so considering the relatively small 6.5 µm pixel pitch.

The method of combining signal from two 11-bit ADCs can be divided into four basic steps:

- At the end of the analogue chain the "Signal" voltage is applied to two independent amplifiers: the high gain amplifier and the low gain amplifier. This results in two separate digital data streams from the sensor.
- In the camera, the FPGA selects which data stream to use on a pixel per pixel, frame by frame basis using a threshold method.
- The data is then corrected for DC offset and gain. Again, this is done on a pixel by pixel basis using the correction data associated with the data stream. The gain corrects for pixel to pixel relative QE, pixel node amplifier and the high and low amplifier relative gains.
- The pixels are then combined into a single 16-bit image for transfer to the PC.

NOTE: Due to the splicing together of the low and high gains, the transition region between them is not seamless but has been optimised as far as possible.

There are two available individual 12-bit gain settings and one dual amplifier 16-bit setting per shutter mode for both fast and slow readout rates, as shown in the below tables. The user maintains the choice of opting to stay with 12-bit single gain channel data if dynamic range is not critical, resulting in smaller file sizes. This in turn offers faster frame rates when continuously spooling through the Camera Link or USB 3.0 interface and writing to hard disk.

Amplifier gain	Electrons/ count	Noise	Signal to noise ratio	Effective well depth (Limited by ADC)
High	Fewer	Lower	Higher	Lower
Low	More	Higher	Lower	Higher

Table 1 - The 'traditional' limiting choice: the mutually exclusive effect of high vs low gain amplifier choice on noise floor and effective well depth.

Amplifier gain (Current Andor SDK / Solis description)	Mode	Sensitivity e⁻/ADU (typical)	Data range	Well depth / e⁻	Spooling file size (per frame)
12-bit (high well capacity)	Rolling shutter	7.5	12-bit	30,000	6 MB
12-bit (low noise)	Rolling shutter	0.28	12-bit	1,100	6 MB
16-bit (low noise and high well capacity)	Rolling shutter	0.45	16-bit	30,000	8 MB

Table 2 - Typical performance of supported gain settings of the Zyla 4.2 PLUS sCMOS

Amplifier gain (Current Andor SDK / Solis description)	Mode	Sensitivity e⁻/ADU (typical)	Data range	Well depth / e⁻	Spooling file size (per frame)
12-bit (high well capacity)	Global shutter/ Rolling shutter	7.5	12-bit	30,000	8 MB
12-bit (low noise)	Global shutter	0.42	12-bit	1,700	8 MB
12-bit (low noise)	Rolling shutter	0.28	12-bit	1,100	8 MB
16-bit (low noise and high well capacity)	Global shutter/ Rolling shutter	0.45	16-bit	30,000	10.5 MB

Table 3 - Typical performance of supported gain settings of the Zyla 5.5 and Neo 5.5 sCMOS